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Comparison of PWM Strategies for Three-Phase Current-fed DC/DC Converters

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ABSTRACT

In this paper, three kinds of PWM strategies for a three-phase current-fed dc/dc converter are proposed and compared in terms of losses and voltage transfer ratio. Each PWM strategy is described graphically and their switching losses are analyzed. With the proposed *PWM C* strategy, one turn-off switching of each bridge switch is eliminated to reduce switching losses under the same switching frequency. In addition, RMS current through the bridge switches is lowered by using parallel connection between two bridge switches and thus, conduction losses of the switches are reduced. Further, copper losses of the transformer are decreased due to the reduced RMS current of each transformer's winding. Therefore, total losses are minimized and the efficiency of the converter is improved by using the proposed PWM C strategy. Digital signal processor (DSP: TI320LF2407) and a field-programmable gate array (FPGA: EPM7128) board are used to generate PWM patterns for three-phase bridge and clamp MOSFETs. A 500W prototype converter is built and its experimental results verify the validity of the proposed PWM strategies.

Keywords: Three-phase dc/dc converter, Three-phase PWM strategy, Losses, Active clamp, Efficiency

1. Introduction

As an interest in clean energy sources has increased significantly in recent years, more effort is being put into fuel-cells, photovoltaic, and wind generation. The rated voltage of a fuel cell is usually lower than 60V [1]. In order to generate 220V ac voltage, at least 400V dc is required for the inverter's input voltage. Therefore, a dc/dc converter is essential for boosting the fuel-cells output voltage to 400V dc voltage [2-4]. At present, the single-phase isolated boost dc/dc converter is widely used to interface low dc voltage with high dc voltage. To enlarge the power transfer capability, the single phase dc/dc converter is extended to the three-phase dc/dc converter [5-8]. Resulted advantages by the three phase configuration are : higher power density caused by three-phase power transfer; a smaller input current and output voltage ripple due to an increase of effective frequencies by a factor of three; lower RMS current through the inverter switches; reduction in size of the reactive (filter) components; better transformer copper and coil utilization. Therefore, this converter is suitable for an interface between a low dc voltage from fuel cells and a high dc voltage for a cascading inverter stage. Fig.1 shows the configuration of the converter and it consists of fuel cells, boost inductor

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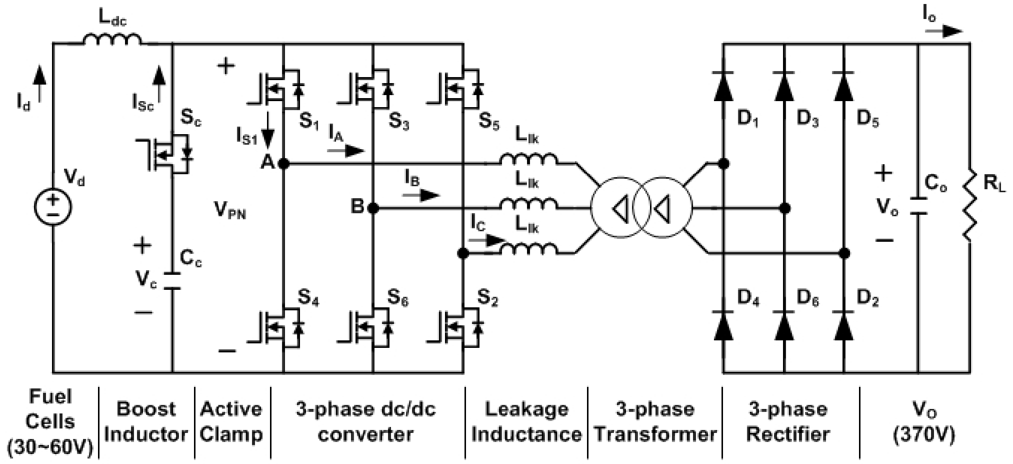


Fig. 1 Three-phase current-fed dc/dc converter with active clamp

active clamp, three-phase dc/dc converter, three-phase transformer, three-phase diode rectifier [9].

2. Comparison of PWM Strategies

Since the system discussed here has a three-phase construction, possible strategies for the three-phase current-fed dc/dc converter are increased. Even though it is the same converter, the voltage transfer ratio and the efficiency could differ according to the PWM strategy applied to the converter. Therefore, the conventional PWM strategy for the three-phase current-fed dc/dc converter is analyzed first. Then, two additional PWM strategies are proposed and compared to find the new PWM strategy that improves the efficiency and increases the voltage transfer ratio.

2.1 PWM A

Fig.2 shows the conventional PWM strategy which exhibits gate signals for S_1~S_6, S_c and its waveforms of input current I_d, bridge switch current I_{s1}, transformer line current I_A, and clamp capacitor current I_{Sc} [9].

Before t_0, all six switches S_1~S_6 are turned on and the boost inductor L_{dc} charges energy from fuel cells V_d.

Mode 1 [t_0~t_1]: At t_0, four switches S_2, S_3, S_4, and S_5 are turned off except S_1 and S_6. The bridge voltage V_{PN} reaches the clamp capacitor voltage V_c and the S_c's body diode conducts the boost inductor current I_d. The current through the leakage inductance L_{lk} increases as a slope determined by a voltage difference between the clamp voltage V_c and the reflected output voltage V_o'. Phase A current I_A starts flowing to the output. To facilitate ZVS for S_c, the switch Sc is turned on before the clamp current I_{Sc} reverses at t_1.

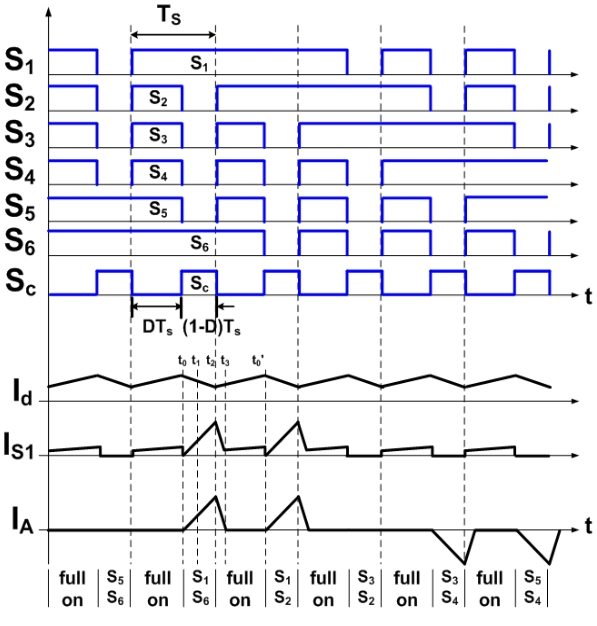


Fig. 2 Waveforms of input current I_d, bridge switch current I_{s1}, and transformer line current I_A with *PWM A*

Mode 2 [t_1~t_2]: The clamp current I_{Sc} reverses and flows through MOSFET S_c. I_{Sc} provides the difference between the increasing I_A and constant boost inductor current I_{dc}.

Mode 3 [t_2~t_3]: At t_2, the active clamp switch S_c is turned off and the energy stored in L_{lk} discharges output capacitances of S_3 and S_4, and then the body diodes of S_3

and S$_4$ begin to conduct. Therefore S_3 and S_4 can be turned on with zero voltage. I_A now decreases at a linear rate determined by the reflected output voltage and the value of L_{lk}. When I_A decreases to the value of the boost inductor current I_d, S_3 and S_4 begin to conduct a half difference between the two currents.

Mode 4 [t_3~t_0']: At t_3, I_A decreases to zero. All switches S_1~S_6 are turned on and the boost inductor L_{dc} charges energy. At t_0', four switches S_3, S_4, S_5, and S_6 are turned off and the same operation repeats again.

When switches are turning off, voltage across the switch falls on the current, resulting in turn-off losses. Switching losses of the bridge can be obtained by the following.

$$P_{Q,S} = \frac{1}{12} V_c I_d t_{sw} f_s \tag{1}$$

Where V_c is a voltage across switch, I_d is an input current, t_{sw} is a switch turn-off transition time, and f_s is a switching frequency. Since the three-phase bridge has six switches, the total switching losses of the bridge switches are,

$$P_{Q,Stotal} = 6 \times P_{Q,S} \tag{2}$$

While current flows through the bridge switches, there are conduction losses because of the on-resistance of the MOSFET switch. Therefore, the conduction losses are obtained by the following.

$$P_{Q,C} = I_{Q,RMS}^2 \times R_{DS} \tag{3}$$

Where, $I_{Q,RMS}$ is a RMS current through a bridge switch, and R_{DS} is an on-resistance of the MOSFET switch. The total conduction losses of the bridge switches are,

$$P_{Q,Ctotal} = 6 \times P_{Q,C} \tag{4}$$

Since the current waveform of the clamp switch is different from those of the bridge switches, the conduction losses of the clamp switch are,

$$P_{Q,Cclamp} = I_{C,RMS}^2 \times R_{DS} \tag{5}$$

Where, $I_{C,RMS}$ is a RMS current through a clamp switch.

The switching losses of the clamp branch switch are,

$$P_{Q,Sclamp} = \frac{1}{2} V_c I_d t_{sw} f_s \tag{6}$$

Therefore, all the losses at the converter switches are,

$$P_{Loss} = P_{Q,Stotal} + P_{Q,Ctotal} + P_{Q,Cclamp} + P_{Q,Sclamp} \tag{7}$$

2.2 PWM B

When switches are turning off, there are turn-off losses. So it is predictable that the efficiency of the converter would be increased by reducing the number of turn-offs. Accordingly, a new PWM strategy is proposed as shown in Fig.3. It is similar to *PWM A* but it differs in that one switching operation is removed to reduce switching losses during switch turn-off transition time. The switch losses could be obtained by the same procedure in the section above.

The main voltage and current waveforms are almost the same as the *PWM A* but the magnitude of the current through bridge switches during the full turn-on interval is different. With *PWM B*, the current through the bridge switches is 1/2 of the input current Id, while *PWM A* flows a third of I_d. Consequently the total switching turn-off losses are the same as with the *PWM A*. Furthermore, the conduction losses increase because the RMS current of each bridge switch is larger than those with the *PWM A*.

2.3 PWM C

In *PWM C*, the basic concept to minimize the switch losses is the same as in *PWM B* but the way to approach is different from *PWM B*. Instead of eliminating one switching operation, just one turn-off operation is canceled as shown in Fig.4. *PWM A* and *PWM B* use two switches at a time while transferring energy to the secondary of the transformer. However, three switches are used at a time with the *PWM C*. As a result, the current waveform of each switch is different because only three bridge switches are turned off after full turn-on. Since the bridge current flows through two ways, each switch connected in parallel takes charge of half of the transformer input current. Therefore, the RMS current of the bridge switch decreases and conduction losses are reduced. In addition, the turn-off losses are reduced to 3/4 of those with *PWM A* by eliminating one turn-off operation at each bridge switch under the same input current.

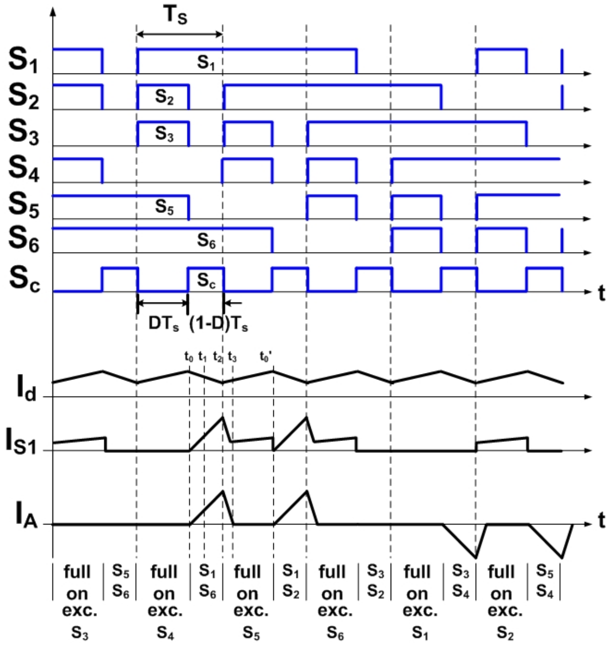


Fig. 3 Waveforms of input current I_d, bridge switch current I_{s1}, and transformer line current I_A with *PWM B*

3. Calculation of Switching Losses

Three-phase current-fed dc/dc converter is simulated with the parameters in Table 1.

Table 1 Parameters used in simulation

Input voltage V_d	30V
Input inductance L_{dc}	330μH
Leakage inductance L_{lk}	7μH
Clamp capacitance C_c	120μF
Output capacitance C_o	470μF
Turn ratio $n(=N_2/N_1)$	4.15
Duty D	0.75
Switching frequency f_s	25kHz
Magnetizing inductance L_m	6mH
Load R_L	270Ω

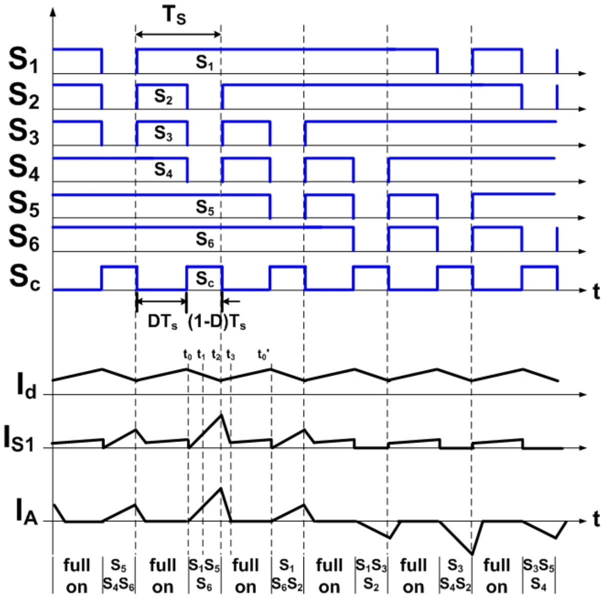
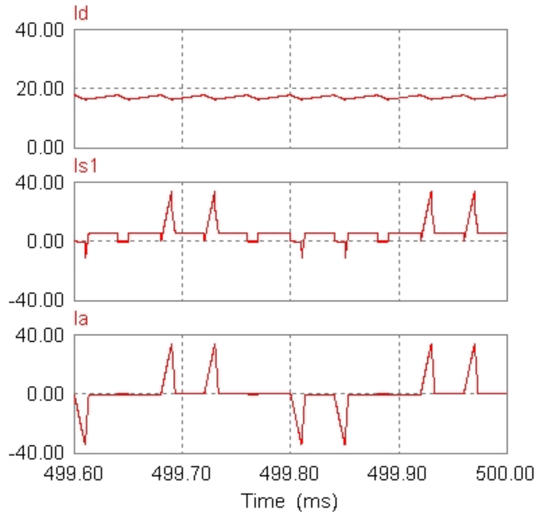
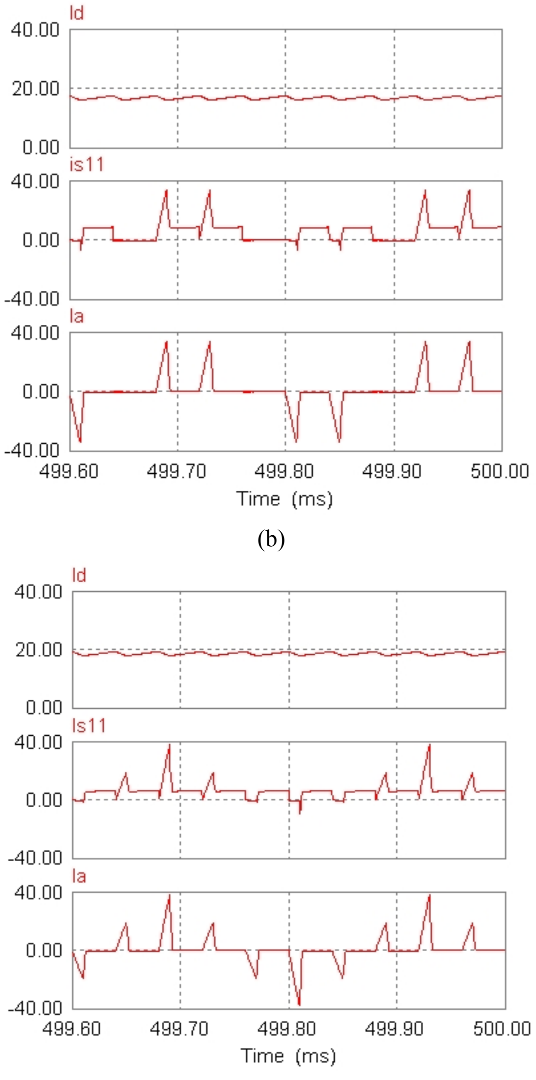


Fig. 4 Waveforms of input current I_d, bridge switch current I_{s1}, and transformer line current I_A with *PWM C*

Fig. 5 shows the input current I_d , bridge switch current I_{S1} , and transformer line current I_A with each PWM strategy. The input current I_d increases during DT_S and decreases during $(1\text{-}D)T_S$. While input current I_d is decreasing, the energy stored in input inductor L is being transferred to the output. The bridge switch current I_{s1} is 1/3 of input current I_d with the *PWM A* and *PWM C*, while 1/2 with the *PWM B*, which is important because the turn-off losses are determined by the current.



(a)



(b)

(c)

Fig. 5 Simulation results - input current I_d, bridge switch current I_{s1}, transformer line current I_A: (a) *PWM A*, (b) *PWM B*, (c) *PWM C*

Table 2 shows the switching losses obtained from the 500W three-phase current-fed dc/dc converter. It appeared that the conduction losses are about 80% of the total switch losses in each case. So it is important to reduce the conduction losses of the switch. With *PWM B*, the switching losses are almost the same as with *PWM A* but the conduction losses are increased compared with the *PWM A*. Consequently, the total losses are increased. However, with the *PWM C*, both conduction and switching losses are decreased. Therefore, it is expected that the efficiency of the converter would be improved just by applying the *PWM C* strategy to the conventional three-phase current-fed dc/dc converter.

Table 2 Comparison of switching losses at each PWM strategy

	Conduction losses(W)		Switching losses(W)		Total losses (W)
	bridge	clamp	bridge	clamp	
PWM A	8.02	0.51	1.28	1.33	11.1
PWM B	9.36	0.51	1.27	1.33	12.4
PWM C	6.53	0.56	1.15	1.20	9.4

4. Implementation and Experimental Results

Fig.6 shows the schematic diagram of PWM switching realization for the three-phase current-fed dc/dc converter. First, the digital signal processor (DSP: TI320LF2407) generates the one full-on signal and six gate PWM signals. Next, the field-programmable gate array (FPGA: EPM7128) modifies the signals from DSP and creates dead-time to facilitate the zero-voltage switching (ZVS) of the bridge switches and clamp switch of the converter. In addition, the gate driver board is added to protect the DSP and FPGA from the surge of the converter.

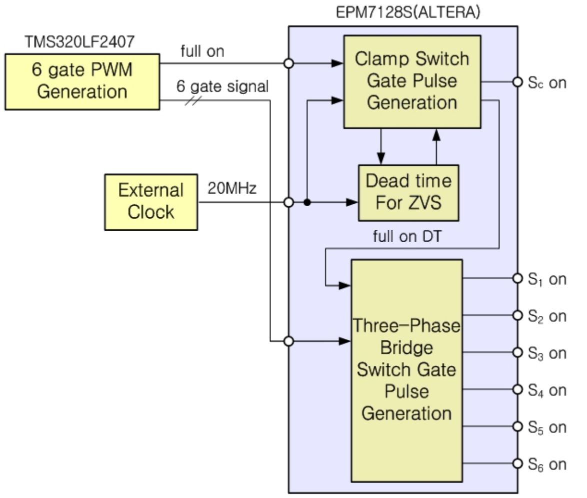


Fig. 6 Generation of gate signal for the bridge and active clamp MOSFET switches

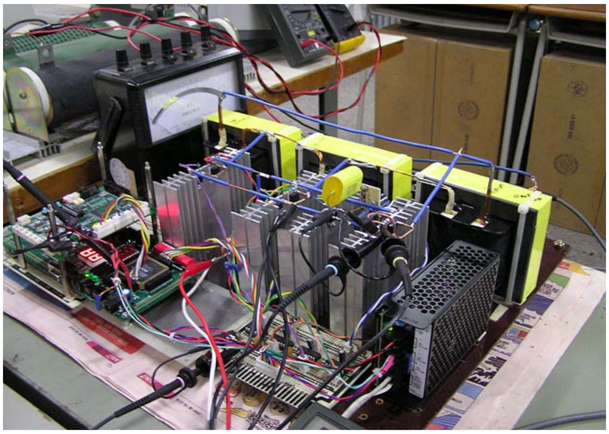
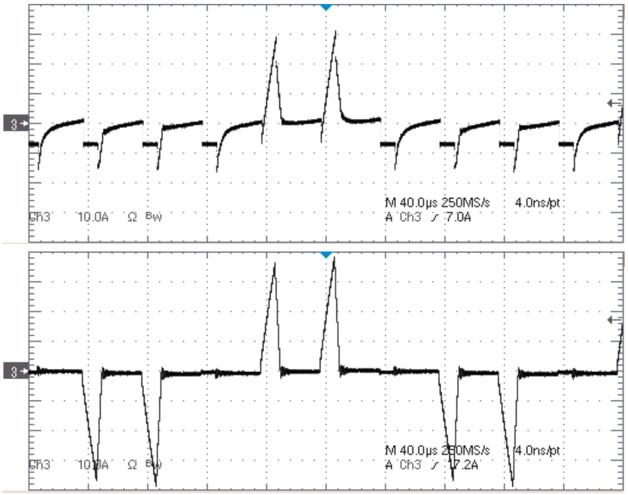


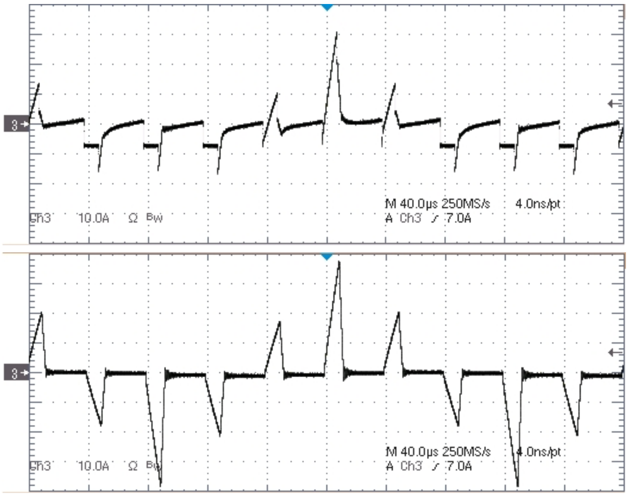
Fig. 7 500W prototype three-phase current-fed dc/dc converter

The 500W prototype three-phase current-fed dc/dc converter is built and tested as shown in Fig.7. It consists of a digital signal processor, a field-programmable gate array board, gate driver board, three-phase bridge and clamp MOSFET, delta-delta wound three-phase transformer, three-phase rectifier and load. The following waveforms are measured under the parameters in Table 1.

Fig. 8 shows the bridge switch current I_{s1} and transformer primary current I_A with the *PWM A* and *PWM C* strategies respectively. The experimental results are in good agreement with the simulation results shown in Fig.5. Two of the bridge switches are turned on during $(1-D)T_S$ with the *PWM A*. However, with the *PWM C*, three of the bridge switches are turned on and the input current Id divided into half flows through two bridge switches in parallel. Therefore, the RMS current of each bridge switch is lowered, which results in the reduction of conduction losses.



(a)



(b)

Fig. 8 Bridge switch current I_{s1} and transformer primary line current I_A (10A/div, 40usec/div): (a) *PWM A*; (b) *PWM C*

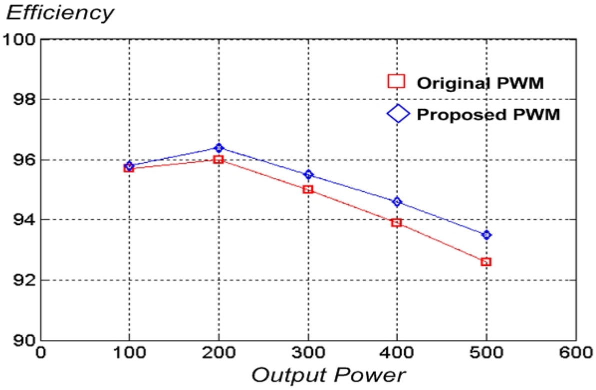


Fig. 9 Efficiency with each PWM strategy

Fig. 9 depicts the efficiency of the converter in *PWM A & C* strategy, where *PWM A* is marked as original PWM and *PWM C* is the proposed PWM in the graph, respectively. In the *PWM C* strategy, switching losses at the switches are reduced by 10% because the number of turn-offs is decreased to 3/4 compared with the *PWM A*. Next, the RMS current of each switch is decreased due to the parallel connection between two bridge switches while transferring the energy to the output. Therefore, conduction losses at switch are reduced. In addition, copper losses at the three-phase transformer are reduced due to the decreased RMS current in each wire. Consequently, overall efficiency is improved by applying the PWM strategy. At 500W load, the converter's efficiency is improved by 1.4%.

5. Conclusions

In this paper, three PWM strategies have been compared and analyzed to improve total efficiency. *PWM A* generates the biggest switching losses because of higher switching during one switching period. To minimize switching losses, *PWM B* and *C* strategies are proposed and tested. *PWM B* has the advantage of a reduced switching number for one period but because of the increased switch current, total switching losses are almost the same. *PWM C* removes just one turn-off of each switch instead of eliminating one switching operation. It decreases both conduction losses and switching losses and results in improving the efficiency of the converter. Simulation and experimental results are addressed to verify the proposed PWM strategy.

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